AFB

Docket No.: 057810-0025

PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Ryosuke USUI, et al.	:	Confirmation Number: 4232
Application No.: 09/985,743	:	Tech Center Art Unit: 2815
Filed: November 06, 2001	:	Examiner: Lee, Eugene

For: SEMICONDUCTOR DEVICE HAVING ELEMENT ISOLATION TRENCH AND METHOD OF FABRICATING THE SAME

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief in support of the Notice of Appeal filed April 25, 2005. Please charge the Appeal Brief fee of $500.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed April 25, 2005, wherein Appellant appeals from the Primary Examiner's rejection of claims 1-3, 6 and 18.

Real Party In Interest

This application is assigned to Sanyo Electric Co., Ltd., by assignment recorded on November 6, 2001, at Reel 012298, Frame 0191.

Related Appeals and Interferences

Appellant is unaware of any related Appeal or Interference.

Status of Claims

Claims 1-3, 6 and 18, which are reproduced in the Appendix, stand twice rejected and are subject to this Appeal. Claims 8-17 stand withdrawn from consideration pursuant to the provisions of 37 C.F.R. § 1.142(b). No other claims are pending.

Status of Amendments

No amendment has been filed since the Office action dated January 25, 2005. Hence, there is no outstanding amendment that has not been entered.

Summary of Claimed Subject Matter

The present claimed subject matter relates to relates to a semiconductor device having an element isolation trench (page 1, lines 6-10 of the specification). An object of the present claimed subject matter is to provide a semiconductor device capable of preventing defective embedding of an insulator in the element isolation trench and improving the withstand voltage (dielectric strength) of an element isolation region (page 3, lines 1-5 of the specification).

Independent claim 1 describes a semiconductor device comprising an element isolation trench 111 that is formed on the main surface of the semiconductor substrate 10. The element isolation trench 111 is substantially filled with an insulator 112. As shown in FIG. 9, the trench width of an upper end of the element isolation trench 111 is larger than the trench width of a bottom surface, while the length of a side surface located between the upper end and an end of the bottom surface is larger than the length of a straight line connecting the upper end and the end of the bottom surface. The side surface of the element isolation trench includes a first side surface 111a located in the vicinity of the upper end of the element isolation trench 111 and is formed to be substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate, as shown in FIG. 9. A second side

surface 111c is located in the vicinity of the bottom surface of the element isolation trench 111 and is formed to be substantially perpendicular to the main surface of the semiconductor substrate. A substantially inclined third side surface 111b connects the first side surface 111a and the second side surface 111c with each other.

Independent claim 18 describes a semiconductor device comprising an element isolation trench 11 formed on the main surface of a semiconductor substrate 10, as shown in FIG. 1. The element isolation trench 11 is substantially filled with an insulator 12. The trench width of an upper end of the element isolation trench 11 is larger than the trench width of a bottom surface. The trench comprises a first side surface 11a located in the vicinity of the upper end of the element isolation trench 11 and is formed to be substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate 10. A second side surface 11c is located in the vicinity of the bottom surface of the element isolation trench 11 and is formed to be substantially perpendicular to the main surface of the semiconductor substrate 10. A third side surface 11b connects the first side surface 11a and the second side surface 11c with each other. The third side surface 11b has a substantially S shape (FIG. 1) or is substantially linearly inclined (FIG. 9) with respect to the main surface of the semiconductor substrate 10.

Grounds of Rejection To Be Reviewed By Appeal

The Rejection:

Claims 1-3, 6 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Okabe et al. (JP 62-252139, hereinafter "Okabe") in view of Kameyama (U.S. Pat. No. 4,472,240, hereinafter "Kameyama").

The Issue Which Arises In This Appeal and Require Resolution by the Honorable Board of Patent Appeals and Interferences is:

Whether claims 1-3, 6 and 18 are unpatentable under 35 U.S.C. § 103 for obviousness predicated upon Okabe in view of Kameyama.

Argument

The rejection of claims 1-3, 6 and 18 under 35 U.S.C. § 103 for obviousness predicated upon Okabe in view of Kameyama

Examiner's Position

The Examiner, at pages 2-3 of the January 25, 2005 Office action (hereinafter "Office action"), stated that Okabe, at Figure 2(E), together with the description at page 3, lines 15-18 of the English language translation, teaches all of the limitations of independent claims 1 and 18, but for an element isolation trench being substantially filled with an insulator. The Examiner asserted that Kameyama, at Figure 11D, teaches an element isolation 511a substantially filled with an insulator 510a. The Examiner concluded that it would have been obvious to modify the device of Okabe in order to have the element isolation trench substantially filled with an insulator in order to isolate semiconductor devices to form an IC or LSI, as suggested by the Kameyama. See page 3 of Office action.

Appellant's Position

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention under any statutory provision always rests upon the Examiner. *In re Mayne*, 41 USPQ2d 1451 (Fed. Cir. 1997); *In re Duel*, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Bell*, 26 USPQ2d 1529 (Fed. Cir. 1993). Appellant submits that this burden has not been established.

Okabe's objective is to eliminate undesirable shapes of the trench isolation walls, including gap 27 and bowling (denting) 29, which Okabe describes as a problem with conventional devices. See page 5, line 8 through page 6, line 15 of the English translation of Okabe. Gap 27 and bowling 29 are depicted at FIG. 2(E) in the Okabe reference. Okabe discloses that it is fairly difficult to fill gap 27 and bowling 29 in the trench and, as a result, the desired insulation resistance value cannot be produced. See page 6, lines 1-11 of the English translation. Moreover, Okabe teaches that the objective is to eliminate the formation of bowling or gaps in the trench during etching. See page 6, lines 12-15. Figure 1(I) of Okabe depicts the desired gradually taper-shaped trench 45 **not** containing any roughness such as bowling formed on the inside wall surface of the trenching. See page 11, lines 14-19 of the English translation. Thus, Appellant submits that the principle operation and objective of Okabe is to eliminate the formation of bowling or gaps in the trench during etching, not to create them. Further, Okabe teaches that the trenches containing bowling or gaps are difficult to fill and the desired insulation resistance value cannot be produced. Okabe clearly teaches that its desired trench shape is a gradually taper-shaped trench 45, as depicted in Figure 1(I).

Independent claim 1 describes a semiconductor device comprising an element isolation trench 111 that is formed on the main surface of the semiconductor substrate 10. The element isolation trench 111 is **substantially filled** with an insulator 112. As shown in FIG. 9, the trench width of an upper end of the element isolation trench 111 is larger than the trench width of a bottom surface, while the length of a side surface located between the upper end and an end of the bottom surface is larger than the length of a straight line connecting the upper end and the end of the bottom surface. The side surface of the element isolation trench includes a first side surface 111a located in the vicinity of the upper end of the element isolation trench 111 and is formed to be substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate, as shown in FIG. 9. A second side

surface 111c is located in the vicinity of the bottom surface of the element isolation trench 111 and is formed to be substantially perpendicular to the main surface of the semiconductor substrate. A substantially inclined third side surface 111b connects the first side surface 111a and the second side surface 111c with each other.

Independent claim 18 describes a semiconductor device comprising an element isolation trench 11 formed on the main surface of a semiconductor substrate 10, as shown in FIG. 1. The element isolation trench 11 is **substantially filled** with an insulator 12. The trench width of an upper end of the element isolation trench 11 is larger than the trench width of a bottom surface. The trench comprises a first side surface 11a located in the vicinity of the upper end of the element isolation trench 11 and is formed to be substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate 10. A second side surface 11c is located in the vicinity of the bottom surface of the element isolation trench 11 and is formed to be substantially perpendicular to the main surface of the semiconductor substrate 10. A third side surface 11b connects the first side surface 11a and the second side surface 11c with each other. The third side surface 11b has a substantially S shape (FIG. 1) or is substantially linearly inclined (FIG. 9) with respect to the main surface of the semiconductor substrate 10.

Appellant submits that there is no reason why one of ordinary skill in the art would modify the trench shape of Okabe since doing so would change the principal operation of Okabe. Indeed, the Examiner's proposed modification would change the principle of operation of Okabe. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). Accordingly, the rejection is not legally viable for at least this reason.

The Examiner is required to show that all the claim limitations are taught or suggested by the references. *In re Royka*, 180 USPQ 580 (CCPA 1974); *In re Wilson*, 165 USPQ 494 (CCPA 1970). However, the secondary reference to Kameyama does not remedy the deficiencies of Okabe. Kameyama, at Figure 11D, fails to disclose or remotely suggest a trench comprising the three side surfaces, each with a specified shape, as required in independent claims 1 and 18. Ergo, even if the applied references are combined as suggested by the Examiner, and Applicants do not agree that the requisite realistic motivation has been established, the claimed invention will not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

Further, it is not clear and the Examiner has not explained how Kameyama would be able to substantially fill Okabe's trench depicted in Figure 2E. Indeed, the shape of Kameyama's trench is not even remotely similar to that depicted in Figure 2E of Okabe. Appellant submits that the Examiner has failed to establish a "thorough and searching" factual inquiry to support the conclusion that a person of ordinary skill in the art would have been motivated to combine the references so as to arrive at the claimed invention. *In re Lee*, 237 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). Appellant submits that the only motivation for the claimed subject matter is Appellant's own disclosure. Appellant's disclosure, however, is forbidden territory for the Examiner to obtain the requisite motivation for combining the applied prior art. *Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985).

Accordingly, Appellant submits that claims 1-3, 6 and 18 are free from the applied art. Appellant, therefore, solicits the Honorable Board to reverse the Examiner's rejection under 35 U.S.C. § 103.

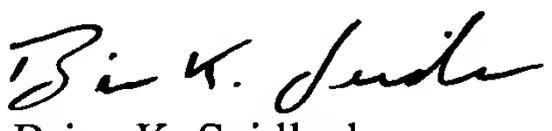
Conclusion

Based upon the arguments submitted supra, Appellant submits that the Examiner's rejection under 35 U.S.C. § 103 is factually and legally erroneous. Appellant, therefore, solicits the Honorable Board to reverse the Examiner's rejection under 35 U.S.C. § 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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CLAIMS APPENDIX

1. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate having a main surface; and

an element isolation trench formed on said main surface of said semiconductor substrate, said element isolation trench being substantially filled with an insulator, wherein

the trench width of an upper end of said element isolation trench is larger than the trench width of a bottom surface while the length of a side surface located between said upper end and an end of said bottom surface is larger than the length of a straight line connecting said upper end and said end of said bottom surface, and

said side surface of said element isolation trench includes:

a first side surface located in the vicinity of said upper end of said element isolation trench and formed to be substantially perpendicular to and extending downwardly from said main surface of said semiconductor substrate,

a second side surface located in the vicinity of said bottom surface of said element isolation trench and formed to be substantially perpendicular to said main surface of said semiconductor substrate, and

a substantially inclined third side surface connecting said first side surface and said second side surface with each other.

2. (Original) The semiconductor device according to claim 1, wherein

the section of at least a central portion of said side surface of said element isolation trench exhibits a curved shape having an angle of inclination gradually steepened toward a downward direction perpendicular to said main surface of said semiconductor substrate.

3. (Original) The semiconductor device according to claim 2, wherein

the section of said side surface of said element isolation trench substantially has an S shape.

Claims 4 and 5 (Cancelled)

6. (Previously Presented) The semiconductor device according to claim 1, wherein

the third side surface is linearly inclined with respect to the main surface of the semiconductor substrate.

7. (Canceled)

8. (Withdrawn) A method of fabricating a semiconductor device comprising steps of:

forming an etching mask on a prescribed region of a main surface of a semiconductor substrate; and

forming an element isolation trench by etching said semiconductor substrate through said etching mask, wherein

said step of forming said element isolation trench includes a step of forming said element isolation trench under an etching condition more readily forming a sidewall protective film in an opening of said semiconductor substrate than an etching condition for forming an element isolation trench having a side surface substantially perpendicular to said main surface of said semiconductor substrate and under such an etching condition that etching gas self-controllably reduces a reduction ratio of the trench width due to reduction of an etching area following reduction of the trench width when performing etching to gradually reduce the width of said element isolation trench.

9. (Withdrawn) The method of fabricating a semiconductor device according to claim 8, further comprising steps of:

forming a silicon oxide film on said main surface of said semiconductor substrate and thereafter forming a silicon nitride film for defining said etching mask on said silicon oxide film,

anisotropically etching prescribed regions of said silicon nitride film and said silicon oxide film thereby patterning said silicon nitride film and said silicon oxide film, and

also anisotropically etching a surface of said semiconductor substrate when anisotropically etching said prescribed regions of said silicon nitride film and said silicon oxide film thereby forming an opening having a side surface substantially perpendicular to said main surface of said semiconductor substrate,

in advance of said step of forming said element isolation trench.

10. (Withdrawn) The method of fabricating a semiconductor device according to claim 8, wherein

the section of at least a central portion of said side surface of said element isolation trench is formed to exhibit a curved shape having an angle of inclination gradually steepened toward a downward direction perpendicular to said main surface of said semiconductor substrate.

11. (Withdrawn) The method of fabricating a semiconductor device according to claim 10, wherein

the section of said side surface of said element isolation trench is formed to substantially have an S shape.

12. (Withdrawn) The method of fabricating a semiconductor device according to claim 10, wherein

the section of a part of said side surface of said element isolation trench close to said upper end is formed to be substantially perpendicular to said main surface of said semiconductor substrate.

13. (Withdrawn) The method of fabricating a semiconductor device according to claim 10, wherein

the section of a part of said side surface of said element isolation trench close to said bottom surface is formed to be substantially perpendicular to said main surface of said semiconductor substrate.

14. (Withdrawn) The method of fabricating a semiconductor device according to claim 8, further comprising a step of embedding an insulator in said element isolation trench.

15. (Withdrawn) A method of fabricating a semiconductor device comprising steps of:

forming an etching mask on a prescribed region of a main surface of a semiconductor substrate;

forming a first side surface substantially perpendicular to said main surface of said semiconductor substrate by anisotropically etching said semiconductor substrate through said etching mask;

thereafter switching an etching condition to an etching condition more readily forming a sidewall protective film in an opening of said semiconductor substrate for etching said semiconductor substrate thereby forming a second side surface; and

thereafter switching said etching condition to an anisotropic etching condition for anisotropically etching said semiconductor substrate thereby forming a third side surface substantially perpendicular to said main surface of said semiconductor substrate.

16. (Withdrawn) The method of fabricating a semiconductor device according to claim 15, further comprising steps of:

forming a silicon oxide film on said main surface of said semiconductor substrate and thereafter forming a silicon nitride film for defining said etching mask on said silicon oxide film,

anisotropically etching prescribed regions of said silicon nitride film and said silicon oxide film thereby patterning said silicon nitride film and said silicon oxide film, and

also anisotropically etching a surface of said semiconductor substrate when anisotropically etching said prescribed regions of said silicon nitride film and said silicon oxide film thereby forming an opening having a side surface substantially perpendicular to said main surface of said semiconductor substrate,

in advance of said step of forming said element isolation trench.

17. (Withdrawn) The method of fabricating a semiconductor device according to claim 15, further comprising a step of embedding an insulator in said element isolation trench.

18. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate having a main surface; and

an element isolation trench formed on said main surface of said semiconductor substrate, said element isolation trench being substantially filled with an insulator, wherein

the trench width of an upper end of said element isolation trench is larger than the trench width of a bottom surface, the trench comprising:

a first side surface located in the vicinity of said upper end of said element isolation trench and formed to be substantially perpendicular to and extending downwardly from said main surface of said semiconductor substrate,

a second side surface located in the vicinity of said bottom surface of said element isolation trench and formed to be substantially perpendicular to said main surface of said semiconductor substrate, and

a third side surface, connecting said first side surface and said second side surface with each other, which has a substantially S shape or is substantially linearly inclined with respect to the main surface.